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Substitute for form 1449A/PTO				Complete If Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number	10/815,370
(use as many sheets as necessary)				Filing Date	1 April 2004 (herewith)
Sheet	2	of	3	First Named Inventor	Chih C. Yeh
				Group Art Unit	2818
				Examiner Name	PHAN
				Attorney Docket Number	MXIC 1571-1

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
TP	A21	2003/0137873		Kawamura	07-24-2003	
TP	A22	2003/0185055		Yeh et al.	10-02-2003	
	A23					
	A24					
	A25					
	A26					
	A27					
	A28					
	A29					
	A30					
	A31					
	A32					
	A33					
	A34					
	A35					
	A36					
	A37					
	A38					
	A39					
	A40					

FOREIGN PATENT DOCUMENTS						
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		Office ³	Number ⁴			
	B11					
	B12					
	B13					
	B14					
	B15					
	B16					
	B17					
	B18					
	B19					
	B20					

Examiner Signature	Trong Phan	Date Considered	1/6/05
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¹ Unique citation designation number. ² See attached Kinds of U.S. Patent Documents. ³ Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶ Applicant is to place a check mark here if English language Translation is attached.

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Sheet

1

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		Number	Kind Code ² (if known)			
TP	A1	4,959,812		Momodomi et al.	09-25-1990	
	A2	5,270,969		Iwahashi	12-14-1993	
	A3	5,424,569		Prall	06-13-1995	
	A4	5,448,517		Iwahashi	09-05-1995	
	A5	5,515,324		Tanaka	05-07-1996	
	A6	5,644,533		Lancaster et al.	07-01-1997	
	A7	5,768,192		Eitan	06-16-1998	
	A8	6,011,725		Eitan	01-04-2000	
	A9	6,172,907		Jenne	01-09-2001	
	A10	6,215,148		Eitan	04-10-2001	
	A11	6,370,062		Choi	04-09-2002	
	A12	6,436,768		Yang et al.	08-20-2002	
	A13	6,458,642		Yeh et al.	10-01-2002	
	A14	6,487,114		Jong et al.	11-26-2002	
	A15	6,566,699		Eitan	05-20-2003	
	A16	6,614,694		Yeh et al.	09-02-2003	
	A17	6,643,181		Sofer et al.	11-04-2003	
	A18	6,690,601		Yeh et al.	02-10-2004	
	A19	Re. 35,838		Momodomi et al.	07-07-1998	
↓	A20	2002/0179958		Kim	12-05-2002	

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		Office ³	Number ⁴	Kind Code ⁵ (if known)				
TP	B1	JP	09162313A		Atsushi	06-20-1997		
TP	B2	JP	11233653A		Shigeki	08-27-1999		
	B3							
	B4							
	B5							
	B6							
	B7							
	B8							
	B9							
	B10							

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				Filing Date	1 April 2004 (herewith)
				First Named Inventor	Chih C. Yeh
				Group Art Unit	2818
				Examiner Name	PHAN
Sheet	3	of	3	Attorney Docket Number	MXIC 1571-1

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS					
Examiner Initials'	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.			
TP	C1	BLOOM, ILAN, et al., "2-Bit Cell NV Memory Minimizes Chip Area with Less Masks," Nikkei Electronics Asia, January 2002, 11 pages			
	C2	DE BLAUWE, JAN, "Nanocrystal Nonvolatile Memory Devices," IEEE Transactions on Nanotechnology, Vol. 1, No. 1, March 2002, 72-77.			
	C3	HIROSE, M., "Challenges for Future Semiconductor Development," International Microprocess and Nanotechnology Conference, 6 November 2002, 47 pages.			
	C4	LEE, JAE-DUK, et al., "Effects of Floating-Gate Interference on NAND Flash Memory Cell Operation," IEEE Electron Device Letters, Vol. 23, No. 5, May 2002, 264-266.			
	C5	SHIN, YOOCHEOL, et al., "High Reliable SONOS-type NAND Flash Memory Cell with Al2O3 for Top Oxide," Non-Volatile Semiconductor Memory Workshop, 2003, 2 pages.			
	C6	LEE, CHANGHYUN, et al., "A Novel Structure of SiO2/SiN/High k Dielectrics, Al2O3 for SONOS Type Flash Memory," Extended Abstracts of the 2002 International Conference on Solid State Devices and Materials, Nagoya, Japan, 2002, 162-163.			
	C7	YEH, C.C., et al., "PHINES: A Novel Low Power Program/Erase, Small Pitch, 2-Bit per Cell Flash Memory," IEEE IEDM, 2002, 931-934.			
	C8	PRINZ, E.J., et al., "An Embedded 90nm SONOS Flash EEPROM Utilizing Hot Electron Injection Programming and 2-Sided Hot Hole Injection Erase," NVM Workshop 2003, 2 pages.			
	C9	RUDEN, P. PAUL, et al., "Modeling of band-to-band tunneling transitions during drift in Monte Carlo transport simulations," J. Appl. Phys., Vol. 88, No. 3, 1 August 2000, 1488-1493.			
	C10	LEE, CHANG HYUN, et al., "A Novel SONOS Structure of SiO2/SiN/Al2O3 with TaN Metal Gate for Multi-Giga Bit Flash Memories," IEEE 2003, 4 pages.			
↓	C11	CHUNG, STEVE S., et al., "A Novel Leakage Current Separation Technique in a Direct Tunneling Regime Gate Oxide SONOS Memory Cell," IEEE 2003, 4 pages.			

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